## REMARKS

Claims 1, 2 and 4-34 are pending in this application and have been rejected as anticipated by Snyder, U.S. Pat. No. 6,507,214. By this Amendment, claims 1, 4-7, 9, 11, 18, 23, 26, 28 and 30 have been amended, and claims 2, 10, 27 and 29 have been cancelled. Therefore claims 1, 4-9, 11-26, 28 and 30-34 are at issue. Of these, claims 1, 9, 23, 25, 26, 28, 30 and 31 are independent.

### Claims 1-29

By this Amendment, independent claims 1, 9, 23, 25, 26 and 28 have been amended to specify:

> wherein the object circuit is a divided circuit of a hardware module for implementing a function, and wherein the boundary condition includes information of timing control of data supplying to the object circuit so that the object circuit functions as the divided circuit of the hardware module when the object circuit is mapped spatially and/or temporally divided to other divided circuits.

The divided circuit is shown in Figure 2. Details of the boundary condition are described in paragraph [0082], relating descriptions are described in paragraphs [0075] and [0077].

In Snyder, the programmable digital circuit blocks are physically connected. However as claimed in claims 1-29, the divided circuits are virtually connected, that is, the divided circuits are mapped spatially and/or temporally divided to the other divided circuits on the logic circuit region. Therefore timing closure issues are solved for each divided circuit, and the boundary conditions of each divided circuit includes information of timing control of inputting data. This is not taught in Snyder.

### Claims 30-34

By this Amendment, independent claim 30 has been amended to specify:

> the elements respectively include an operation core that performs a logic operation on input data and outputs output data, the operation core including a selector into which a multibit function code for designating the logic operation is inputted and which selects the output data according to the input data as a logic operation element.

The element as claimed in claims 30-34 includes an operation core that includes a selector to which a multibit function code is input then output data is selected according to the input data as a logic operation element. Details are shown in Figures 13-16 and relating descriptions such as paragraphs [0097]-[0100]. That is, logic is reconfigured in the logic operation element level such as AND gate, NAND gate and others as shown in Fig 16.

In Snyder, the selectable logic circuit 30 includes a plurality of logic gates (see lines 59-60 of column 5) and functions are changed in module level such as PWM, CRC, PRS, UART, SPI (see lines 13-34 of column 6).

Snyder neither discloses nor suggests a configurable logic circuit that includes elements with the operation core that is reconfigurable in the logical operation element level (logic gate level).

In view of the above amendments, Applicant submits the pending application is in condition for allowance. Should the Examiner wish to discuss the foregoing, or any matter of form, in an effort to advance this application toward allowance, the Examiner is urged to telephone the undersigned at the indicated number

Dated: October 5, 2011

Respectfully submitted,

By /Thomas K. Stine/
Thomas K. Stine
Registration No.: 32,310
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive
Suite 6300
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant